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1. A stacked-gate flash memory cell having a floating Poly-Si gate with multiply connected surfaces of different shapes comprising:

providing a semiconductor substrate;

a floating Poly-Si gate with multiply connected surfaces of different shapes;

an inter-poly dielectric layer over said floating Poly-Si gate; and

a Poly-Si control gate over said inter-poly dielectric layer.

2. A stacked-gate flash memory cell of claim 1, wherein said floating Poly-Si gate has a thickness between about 1900 to 2100 Å.

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3. A stacked-gate flash memory cell of claim 1, wherein said multiply connected surfaces have a depth between about 900 to 1100 Å.

4. A stacked-gate flash memory cell of claim 1, wherein said different shapes are rectangular and triangular.

5. A stacked-gate flash memory cell of claim 1, wherein said inter-poly dielectric layer is oxide-nitride-oxide having a thickness between about 150 to 250 Å.

6. A stacked-gate flash memory cell of claim 1, wherein said Poly-Si control gate has a thickness between about 1500 to 2000 Å.

7. A method of forming a stacked-gate flash memory having a floating Poly-Si gate with multiply connected surfaces of different shapes comprising the steps of:

providing a semiconductor substrate;

forming a gate-oxide layer over said substrate;

forming a first polysilicon layer over said gate-oxide layer;

forming multiply connected surfaces of different shapes in said first polysilicon layer;

forming a first polysilicon (Poly-Si) floating gate having said surfaces of different shapes;

forming an inter-poly oxide layer over said floating Poly-Si gate having said surface of different shapes; and

forming a Poly-Si control gate over said floating Poly-Si gate.

8. The method of claim 7, wherein said gate-oxide layer has a thickness between about 70 to 150 Å.

9. The method of claim 7, wherein said first polysilicon layer has a thickness between about 1900 to 2100 Å.

10. The method of claim 7, wherein said multiply connected surfaces have a depth between about 900 to 1100 Å.

11. The method of claim 7, wherein said different shapes are rectangular and triangular.

12. The method of claim 7, wherein said inter-poly dielectric layer is oxide-nitride-oxide having a thickness between about 150 to 250 Å.

13. The method of claim 7, wherein said Poly-Si control gate has a thickness between about 1500 to 2000 Å.

14. A method of forming a stacked-gate flash memory cell having a step-shaped floating Poly-Si gate comprising the steps of:

providing a semiconductor substrate;

forming a gate-oxide layer over said substrate;

forming a first polysilicon layer over said gate-oxide layer;

forming a mask layer over said pad-oxide layer;

patterning and forming an opening in said mask layer to define a floating gate region in said substrate;

forming spacers in said opening and to expose said first polysilicon layer in said opening;

performing a partial etch of said first polysilicon layer

exposed in said opening to form a step-shaped surface on said first polysilicon layer;

removing said spacers and said mask layer;

forming a step-shaped inter-poly dielectric layer over said substrate including said floating Poly-Si gate with said step-shaped surface;

forming a second polysilicon layer over said step-shaped inter-poly dielectric layer;

removing said second polysilicon layer and underlying said inter-poly oxide layer from said substrate, excluding from regions over floating Poly-Si gate, thus forming a Poly-Si control gate having step-shaped surface corresponding to said floating Poly-Si gate with step-shaped surface; and

performing ion implantation to form source and drain of said stacked-gate flash memory cell.

15. The method of claim 14, wherein said forming said first polysilicon layer is accomplished using an LPCVD method employing silane SiH_4 as a silicon source material at a temperature range between about 600 to 700 °C.

16. The method of claim 14, wherein said first polysilicon layer has a thickness between about 1900 to 2100 Å.

17. The method of claim 14, wherein said spacer is tetraethyl orthosilicate oxide having a thickness between about 1000 to 2500 Å.

18. The method of claim 14, wherein said partial etch of said first polysilicon layer to form said step-shaped surface is accomplished with gases $HBr+Cl_2$.

19. The method of claim 14, wherein said forming said step-shaped inter-poly oxide is accomplished by forming an oxide-nitride-oxide (ONO) layer having a thickness between about 150 to 250 Å.

20. The method of claim 14, wherein said second polysilicon layer has a thickness between about 1500 to 2000 Å.